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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,532	08/20/2001	Farid N. Najm	SIME:007	5826

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Maximilian R. Peterson
O'KEEFE, EGAN & PETERMAN
Building C, Suite 200
1101 Capital of Texas Highway South
Austin, TX 78746

EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	4

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/933,532	NAJM ET AL.
	Examiner	Art Unit
	Jason Proctor	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/18/2001.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been rejected.

Priority

2. Applicant's request for priority under 35 U.S.C. §119(e) in reference to US Patent Application 60/229,825 is acknowledged.

3. It has come to the attention of the examiner that the applicant Farid N. Najm has authored or co-authored many scientific papers that read on some of the claimed subject matter, for example:

1. Joseph N. Kozhaya, Farid N. Najm, "Accurate power estimation for large sequential circuits", Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design, 1997
2. Subodh Gupta, Farid N. Najm, "Power macromodeling for high level power estimation", Proceedings of the 34th annual conference on Design automation - Volume 00, 1997
3. Kavel M. Büyükşahin, Farid N. Najm, "High-level power estimation with interconnect effects", Proceedings of the 2000 international symposium on Low power electronics and design, 2000

4. In any response, the applicant is requested to submit any other papers authored by the applicant that could be considered prior art.

Drawings

5. The drawings are objected to because they do not have satisfactory reproduction characteristics. See 37 CFR § 1.84(l). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. For example, Figures 8A and 8B drawn by a process such that the lines and reference characters are not legible after being reproduced. Figures 3, 4A, 4B, 5A, 5B, 6A, 6B, 6C, 10A, 10B, and 10C are cause for similar objections.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 21-30 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claims 21-30 are directed toward a method of characterizing a circuit according to a model of its operation. The method is an abstract algorithm and requires no tangible embodiment nor does it require interaction with an existing circuit. Thus the method is a process that consists solely of the manipulation of an abstract idea and therefore nonstatutory. See MPEP § 2106 (II)(A).

9. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3-10, 13-20, and 23-30 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 3, 13, and 23 recite limitations including the phrase "a substantially capacitive load" and therefore indefinite. While the term "substantially" has been found to be broad in some circumstances, in this case the disclosure provides no basis for determining whether a load is substantially capacitive. See MPEP § 2173.05(b).

13. Claims 4, 14, and 24 recite limitations including the phrase "an effective input capacitance" and therefore indefinite. The disclosure provides no indication as to how one would differentiate "an effective input capacitance" from an ordinary input capacitance nor what order of capacitance is required for an input to be distinguished as "an effective input capacitance". See MPEP § 2173.05(b).

14. Claims not specifically mentioned are rejected by virtue of their dependency.

Claim Interpretation

15. In the interest of compact prosecution, examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

16. Regarding claims 3, 13, and 23, the phrase "a substantially capacitive load" is interpreted as "a capacitive load".

17. Regarding claims 4, 14, and 24, the phrase "an effective input capacitance" is interpreted as "an input capacitance".

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by McNelly et al., US Patent No. 5,625,803.

20. Regarding claim 1, McNelly et al. teaches a system that characterizes multiple power-supply circuits (column 2, lines 42-46; column 9, line 61 – column 10, line 10; column 10, lines 49-55) comprising

a computer for characterizing energy attributes of a circuit (column 3, lines 19-27; column 2, lines 33-37),

the circuit includes a cell (column 2, lines 42-46),

the cell couples to a plurality of power supplies and has one or more outputs that drive, respectively, one or more loads (column 10, lines 49-55; column 16, lines 6-20),

the computer is configured to characterize a dynamic energy attribute of each of the power supplies (column 9, line 61 – column 10, line 10; column 16, lines 6-27),

to characterize a dynamic energy attribute of the one or more loads (column 16, lines 6-27),

to calculate an overall dynamic energy attribute for the plurality of power supplies (column 2, line 56 – column 3, line 10),

to determine an overall dynamic energy attribute for the one or more loads (column 2, line 56 – column 3, line 10),

and to compute a dynamic energy attribute of the cell (column 2, line 56 – column 3, line 10).

21. Regarding claim 2, McNelly et al. teaches that a dynamic energy attribute of each of the power supplies is characterized by multiplying a voltage across the respective power supply by a charge flowing through the respective power supply (column 15, lines 39-65).

22. Regarding claim 3, McNelly et al. teaches that the one or more loads comprise a capacitive load (column 5, lines 44-56; column 13, lines 35-53).

23. Regarding claim 4, McNelly et al. teaches that the one or more loads comprise an input capacitance of a circuit coupled to the respective output of the cell (column 5, lines 7-56; column 9, line 35 – column 10, line 10; column 13, lines 35-53).

24. Regarding claim 5, McNelly et al. teaches that the one or more loads further comprise a capacitance of an interconnect structure coupled to the respective output of the cell (column 5, lines 7-56; column 17, lines 16-34).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 2 and 6-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McNelly et al as applied to claims 1 - 5 above, further in view of official notice.

27. Claim 2 recites characterizing a dynamic energy attribute of a power supply by multiplying a voltage across the power supply by a charge flowing through the power supply. Electric current is defined as charge flowing through a conductor (See Cathy & Nasar, page 1). Electric power is defined as voltage times current (See Cathy & Nasar, page 2).

28. Official notice is taken that multiplying voltage by current is a method known in the art for calculating power and could be easily incorporated into the invention of McNelly et al. It would have been obvious to a person of ordinary skill in the art of electrical engineering at the time of applicant's invention to characterize a power supply in terms known in the art such as electrical power.

29. Claim 6 recites characterizing the dynamic energy attribute of a load by multiplying one half of the capacitance of the load by a square of a voltage across the load.

30. Official notice is taken that a known method for characterizing stored electrical energy is to multiply one half the capacitance by the square of the voltage (See Cathy & Nasar, page 5). It would have been obvious to a person of ordinary skill in the art of electrical engineering at the time of applicant's invention to characterize a capacitive

load in terms of stored energy using methods known in the art. The limitations of claim 6 are well known in the art and could be easily incorporated into the power calculation of McNelly et al.

31. Claim 7 recites characterizing charge flow of a power supply by integrating with respect to time a current flowing through the power supply.

32. Official notice is taken that using integration to find the total from a function that represents the instantaneous amount dependent upon time is well known in the art (See "Integral", from Wikipedia). It would have been obvious to a person of ordinary skill in the art at of electrical engineering at the time of applicant's invention to characterize a total charge flow through a power supply by integrating a function that represents the instantaneous charge flow dependent on time. The limitations of claim 8 are well known in the art and could easily be incorporated into the power calculation of McNelly et al.

33. Claim 8 recites characterizing a static energy attribute of a power supply by multiplying a voltage across the power supply by a charge flowing through the power supply.

34. Official notice is taken that electric current is defined as charge flowing through a conductor (See Cathy & Nasar, page 1). Electric power is defined as voltage times current (See Cathy & Nasar, page 2). It would have been obvious to a person of ordinary skill in the art of electrical engineering at the time of applicant's invention to characterize a power supply in terms known in the art such as electrical power. Multiplying voltage by current is a method known in the art for calculating power and could be easily incorporated into the power calculation of McNelly et al.

35. Regarding claim 9, McNelly teaches that the cell includes complimentary metal oxide semiconductor circuitry (column 13, lines 35-53). CMOS is a known acronym for "complimentary metal oxide semiconductor" (See "CMOS", Microsoft Computer Dictionary).

36. Claim 10 recites characterizing a circuit that includes at least one positive power supply and at least one negative power supply.

37. Official notice is taken that circuits that include at least one positive power supply and at least one negative power supply are well known in the art, such as those involving operational amplifiers (See "Operational amplifier", from Wikipedia). It would have been obvious to a person of ordinary skill in the art of electrical engineering at the time of applicant's invention to characterize an electronic circuit that includes at least one positive power supply and at least one negative power supply. The invention of McNelly et al. provides for circuits with multiple voltage sources (column 10, lines 49-55). While McNelly et al. does not specifically disclose whether their invention simulates and characterizes both positive and negative voltage sources, it would be advantageous to do so when working in CMOS circuits. The ability to support multiple power supplies of McNelly et al. could easily be modified to characterize at least one positive power supply and at least one negative power supply.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Sarin, US Patent No. 5,692,160 shares a common assignee with McNelly et al. and discloses an invention similar to that used above to reject the claims based on prior art.

Omori et al. US Patent No. 5,473,548; Lai, US Patent No. 5,768,130; and Olson et al. US Patent Nos. 5,949,689 and 6,480,815 disclose an invention similar to the instant application but without support for multiple power supplies.

Roche, US Patent No. 6,430,518 discloses a system to monitor and control circuits comprising multiple loads and power supplies.

Moriwaki et al. US Patent No. 6,490,715 discloses simulation of a circuit that controls a power supply.

Farid N. Najm (1994), Jose Monteiro & Srinivas Devadas (1995), Srinivas Devadas & Sharad Malik (1995), and Massoud Pedram (1996) teach a variety of power estimation techniques and strategies for minimizing power consumption in integrated circuit designs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (703) 305-0542 or (571) 272-3713 beginning in October 2004. The examiner can normally be reached on 8am-4pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704 or (571) 272-3716

beginning in October 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER